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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/663,774	09/17/2003	Kyoung Mook Lee	8733.915.00-US	1766

7590 03/23/2005  
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EXAMINER

AKKAPEDDI, PRASAD R

ART UNIT PAPER NUMBER

2871

DATE MAILED: 03/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/663,774

Applicant(s)

LEE ET AL.

Examiner

Prasad R. Akkapeddi

Art Unit

2871

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

**DETAILED ACTION**

***Claim Rejections - 35 USC § 103***

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-5, 7-19, 23-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song et al. (Song) (U.S. Patent No. 6,215,541) in view of Ozaki et al. (Ozaki) (U.S. Patent No. 6,184,947).

As to claims 1 and 8: Song discloses an array substrate for a liquid crystal display device (Fig. 5) a substrate (100), a gate line (20) and a thin film transistor having a gate electrode (21), a source electrode (61), a drain electrode (62) and an active layer (40) formed over the substrate (100), an interlayer insulating layer (30) formed on the thin film transistor, a first gate redundancy line (64) (Fig. 5) formed on the interlayer insulating layer, and connected electrically with one of the gate electrode (21), the gate line (20), and both the gate electrode (20) and gate line (20) through a first gate contact hole (75). Song also discloses a passivation layer (70) provided on the first gate redundancy line and the interlayer insulating layer (30) and a pixel electrode (66) electrically connected with the drain electrode through the drain contact hole formed in the passivation layer (Fig. 17b).

Song teaches that the gate redundancy line is made of chromium, molybdenum or molybdenum alloy. However, Song does not teach that the gate redundancy line is formed of the same material as one of the source and drain electrodes, which are made from a semiconductor material as, can be seen from Fig. 7.

Ozaki in disclosing thin film transistor matrix with repair bus lines teaches that the gate line (GL) can also be made of a semiconductor layer having a high impurity concentration (col. 3, lines 62-64).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the gate line made from a semiconductor material (as taught by Ozaki) in place of metals such as chromium, molybdenum or molybdenum alloy (as taught by Song) to avoid pin holes that might be formed in the metal layers and to repair any breakage in the metal layer (col. 2, lines 49-56).

As to claims 2-5, 7 and 9-13: Song teaches the thin film transistor as a bottom gate thin film transistor, the first gate contact hole (75) is formed passing through the interlayer insulating layers and also teaches a second gate contact hole for connection of the first gate redundancy line with the gate line (Fig. 5) and (col. 6, lines 1-9). Ozaki teaches that the thin film transistor can also be a top gate thin film transistor (Fig. 1D).

As to claims 14 and 24: Song discloses the method of fabricating the array substrate for a liquid crystal display in (col. 11, lines 13-67), (col. 12, lines 1-67)

and (col. 13, lines 1-10). The method comprises forming a gate line and a gate electrode on a substrate, forming an interlayer insulating layer on the gate line and the gate electrode, forming a thin film transistor with the gate electrode, a source electrode, a drain electrode, and an active layer, forming a first gate redundancy line on the interlayer insulating layer electrically connected with one of the gate electrode, the gate line, and both the gate electrode and gate line through a first gate contact hole, forming a passivation layer on the first gate redundancy line and the interlayer insulating layer; and forming a drain contact hole in the passivation layer, and forming a pixel electrode connected electrically with the drain electrode through the drain contact hole.

As to claims 15-19, 23 and 25-30: Song teaches the formation of the thin film transistor as a bottom gate thin film transistor, the first gate contact hole (75) is formed passing through the interlayer insulating layers and also teaches a second gate contact hole for connection of the first gate redundancy line with the gate line (Fig. 5) and (col. 6, lines 1-9). Ozaki teaches that the formation of the thin film transistor as a top gate thin film transistor (Fig. 1D).

3. Claims 6 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Song in view of Ozaki as applied to claims 1 and 14 above, and further in view of Huh et al. (Huh) (U.S. Patent No. 6,307,216).

As to claims 6 and 20-22: Neither Song nor Ozaki teach the formation of a second gate line.

Huh in disclosing a thin film transistor panel for liquid crystal displays, teaches the use of a second gate line and electrical connection to the first gate line (col. 2, lines 26-43) and (col. 3, lines 45-67). Huh also teaches the contact holes (C1, C2 and C3) formed in the passivation film (30) and the material of the connect pattern is made of the same material as the pixel electrode (col. 4, lines 23-35).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to adapt the second gate line and its electrical connection to the first gate line as disclosed by Huh to the devise of Song in view of Ozaki to provide a redundancy line structure used for effectively repair disconnection defects without introducing additional steps and for preventing short-circuited defects between the upper and the lower substrates and between adjacent pixels (col. 1, lines 45-55).

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. (a) Hyun (U.S. Patent No. 5,856,854) and (b) Salisbury (U.S. Patent No. 5,303,074).

Art Unit: 2871

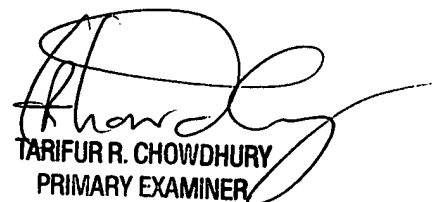
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prasad R. Akkapeddi whose telephone number is 571-272-2285. The examiner can normally be reached on 7:00AM to 5:30PM M-Th.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert H. Kim can be reached on 571-272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Prasad R Akkapeddi, Ph.D  
Examiner  
Art Unit 2871

BRA  
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TARIFUR R. CHOWDHURY  
PRIMARY EXAMINER